REMARKS

The Examiner has rejected claims 1, 11 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,630,953 to Toyoda et al. in view of U.S. Patent 5,926,216 to Nobuoka, and further in view of U.S. Patent 5,892,551 to Uematsu. The Examiner has further rejected claims 2-7 under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al. in view of Nobuoka and Uematsu, and further in view of U.S. Patent 6,380,985 to Callahan. In addition, the Examiner has rejected claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al. in view of Nobuoka, Uematsu and Callahan, and further in view of U.S. Patent 6,489,998 to Thompson et al. Finally, the Examiner has rejected claim 9 under 35 U.S.C. 103(a) as being unpatentable over Toyoda et al. in view of Nobuoka and Uematsu, and further in view of Thompson et al.

The Toyoda et al. patent discloses a flicker control imaging apparatus, in which the mean luminance of two areas of a picture signal divided by a movable boundary is detected (col. 1, lines 43-46). The flicker in each of the two areas is corrected to derive a correction-resultant area in response to the mean luminance (col. 1, lines 52-53). The two correction-resultant areas are then combined into a correction-resultant picture (col. 1, lines 55-57).

Nobuoka discloses an image sensing apparatus capable of sensing an image with high signal to noise ratio (col. 2, lines 3-5). The image sensing apparatus includes an optical focusing system for focusing an image on a photo-sensing surface, photoelectric

conversion means for converting an optical image to generate an electric signal, integration means for integrating the electric signal, integration control means, and output means for generating the image signal (col. 2, lines 6-22). Nobuoka shows a predetermined luminance value, temporarily storing image signals in a frame memory, and feeding stored images back to an adder (col. 4, lines 64-68). The image data is added with a newly inputted signal and the added signal is stored in the first frame memory until the luminance level of the image signal stored in a first frame memory is greater or equal to the predetermined luminance value (col. 5, lines 4-9).

Uematsu patent discloses a flicker reducing circuit which contains two delay units. One of these units delays composite data processed in the display processing unit by a process time in the vertical low-pass filter, and then outputs the result. Another of these units receives character image data formed of only character data, among data processed in the display processing unit, and delays the data by a processing time in the vertical low-pass filter, then outputs the result (col. 1, lines 36-42). Uematsu's circuit reads character data and composite data out of a memory unit to display them (col. 1, lines 31-32).

35 U.S.C. 103(a) states "(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the

time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made."

Applicants submit, however, that a prerequisite is that each of the elements, as claimed, need to be shown in the prior art, or shown to be obvious by in light of the prior art.

The Examiner has indicated that Toyoda et al. discloses "a light modulation removal means (combination of elements 14, 15, 17A, 17B, 17C, 17D, 19, 20, figure 2, column 5, lines 1-50, correcting a flicker) between the processing unit and the end processing unit for removing light modulation between different fields of the picture, by averaging images having the same light modulation (calculating mean brightness, column 3, lines 55-59; column 4, lines 40-47)."

Applicants submit that the Examiner is mistaken. In particular, while Toyoda et al. discloses calculating the mean brightness, this is done for each field, i.e., in the four divided areas of each field. Hence, there is no disclose of "averaging images having the same light modulation".

The Examiner further states "Toyoda et al. fails to specifically disclose averaging stored images. However Nobuoka teaches an image sensing apparatus, which stores image in frame memory 8 before transmitting images to luminance detector 9 (figure 1, column 4, line 58 - column 5, line 10).

Applicants submit that while Nobuoka arguably discloses storing images in a frame memory, this combined with Toyoda et al.

does not disclose or suggest the limitation "averaging images having the same light modulation". Rather, the only thing that is disclosed by the combination of Toyoda et al. and Nobuoka is that "calculating the mean brightness, this is done for each field, i.e., in the four divided areas of each field" and that the image sensing apparatus includes a frame memory for storing at least one field of the image.

The Examiner now adds "Toyoda et al. and Nobuoka fail to specifically disclose wherein said light modulation removal means further comprises a motion detector for detecting the effect of motion on a scene. However, Uematsu teaches a flicker reducing circuit 10 consists of a noise reducer 11 in which mosquito noise are removed through motion detection between a previous frame and the following frame, and a motion detection signal in motion detection (figure 1, column 6, lines 49-67)."

Applicants submit that while Uematsu teaches a flicker reducing circuit consisting of a noise reducer in which mosquito noises are removed through motion detection between a previous frame and the following frame, and a motion detection signal in motion detection, Uematsu fails to teach or suggest a means for removing light modulation by averaging stored images having the same light modulation, "wherein said light modulation removal means further comprises a motion detector for detecting the effect of motion on a scene" as is the subject matter of Applicants' claim 1. Rather, Uematsu merely discloses motion detection without any relation to its use in removing light modulation.

The Callahan patent discloses resizing and anti-flicker filtering in reduced-sized video images which filters a data stream to produce a reduced-size display image while minimizing flicker (col. 1, lines 46-49). The Callahan system contains a resizing and filtering component to remove and resize two fields of interlaced scan lines by averaging pairs of sequential scan lines, thereby producing averaged line pairs (col. 5, lines 9-11). The component then filters the averaged line pairs to remove interlace flickering (col. 5, lines 13-17).

The Examiner now states "Toyoda et al., Nobuoka and Uematsu fail to specifically disclose the light modulation removal means comprise adaptive fading means for fading between one field and at least n fields, whereby n is the repetition pattern of light modulation. However, Callahan discloses a system for resizing and anti-flicker filter in reduced-size video images, in which after one field is output and begins to fade, the other field is output to replace the fading first field. This alternating pattern results in a continual refreshing of the displayed image (column 4, lines 33-45).

Applicants submit that the Examiner is mischaracterizing the Callahan patent. In particular, while Callahan "mentions" the term "fading", Callahan is merely describing the process of displaying consecutive fields of interlaced video lines where once a line on a cathode ray tube is energized, this line will fade unless re-energized. In interlace scanning, the intervening lines of an ensuing field are displayed prior to the fading of the lines

of the preceding field. However, there is no disclosure or suggestion in Callahan of "adaptive fading means for fading between one field and at least n fields, whereby n is the repetition pattern of light modulation".

Furthermore, Applicants submit that Callahan does not supply that which is missing from Toyoda et al., Nobuoka and Uematsu, i.e., "a light modulation removal means between the processing unit and the end processing unit for removing light modulation between different fields of the picture, by averaging stored images having the same light modulation, wherein said light modulation removal means further comprises a motion detector for detecting the effect of motion on a scene".

Claim 8 includes the limitation "the light modulation removal means comprise means to correct consecutive images to the same temporal position using motion compensated conversion techniques prior to the averaging".

The Thompson patent discloses a method and apparatus for deinterlacing digital video images. According to the Examiner, "Thompson et al. discloses an apparatus for deinterlacing digital video images comprises a deinterlacing processor which generates the interlaced video stream having reduced motion artifacts (correct consecutive images, column 3, lines 5-8)."

It is unclear to Applicants how the Examiner comes to this conclusion in that the indicated section of Thompson states "The deinterlacing processor is operable to perform frequency analysis upon the received interlaced video stream in order to generate the

video stream having reduced motion artifacts." However, regardless of the Examiner's interpretation, there is no disclosure of "means to correct consecutive images to the same temporal position", let alone that the means uses motion compensated conversion techniques.

In view of the above, Applicants believe that the subject invention, as claimed, is not rendered obvious by the prior art, and as such, is patentable thereover.

Applicants believe that this application, containing claims 1-9 and 11, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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